It is noted that the previously made Restriction Requirement has been made final. Nonelected claims 2 - 11 have been withdrawn from further consideration.

The objection to the drawings by the Patent Office Draftsman has been noted. In response thereto, the Applicant is filing correct formal drawings.

On page 2 of the Office Action, the Patent Examiner has rejected claim 1 under 35 U.S.C. 103 as being unpatentable over *Wilson et al U.S. Patent No. 6,284,384* and *Krishna Vepa et al. EPA Patent* No. 684,634.

On page 3 of the Office Action, the Patent Examiner has contended as follows. The Patent Examiner has admitted that *Wilson* does not specifically describe the front surface of the wafer prior to the deposition of epitaxial layer as having a surface roughness of 0.05 to 0.29 nm RMS, measured by AFM on a 1 μm by 1 μm reference area. The Patent Examiner then agrees that *Vepa* patent from the same field of endeavor, describes a polishing method that produces an average surface roughness of not greater than 1.0 nm Ra to produce a wafer with improved surface roughness with reduced haze.

The Patent Examiner then concludes that therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to apply *Vepa's* surface roughness parameters to *Wilson's* polishing process to produce the claimed semiconductor wafer.

This rejection is respectfully traversed.

The present invention is directed to a semiconductor wafer with a front surface and a back surface and an epitaxial layer of semiconducting material deposited on the front surface; wherein a surface of the epitaxial layer has a maximum density of 0.14 localized light scatterers per cm^2 with a cross section of greater than or equal to 0.12 μm; and the front surface of the semiconductor wafer, prior to the deposition of the epitaxial layer, has a surface roughness of 0.05 to 0.29 nm RMS, measured by AFM on a 1 μm x 1 μm reference area.

As to the rejection of claim 1, it is pointed out that *Wilson* does not teach all features of the claim. Moreover *Wilson et al.* do not describe that the front surface of the semiconductor wafer, prior to the deposition of the epitaxial layer, having a surface roughness of 0.05 to 0.29 nm RMS, measured by ATM on a 1 μm * 1 μm reference area. Actually,

it's 103 rejection not 102

Wilson et al the primary reference does not mention any roughness values, at all.

On the other hand, the secondary reference *Vepa et al* fails to teach this specific feature. The best mode disclosure of *Vepa et al.* refer to a surface roughness of about 0.5 to 0.8 nm Ra (cf.p.4, lines 34-35 and p.7, claim 10). If this best mode is compared with the claimed invention, i.e. a surface roughness of 0.05 to 0.29 nm RMS, there is still a difference of at least 58%.

Next attention is drawn attention to p.17, second paragraph of the Specification of the present patent application. According to the example mentioned in this paragraph, the roughness of the prepolished wafers was 0.7 nm RMS. This value corresponds fairly close to the roughness which is taught by *Vepa et al.* (cf. p.6, lines 13-14). However, according to the present invention the roughness achieved by polishing of the wafer is further improved to the claimed range of 0.05 to 0.29 nm RMS by subjecting the wafer to a pretreatment which is described on p. 17 in the last paragraph.

The Patent Examiner is correct in stating that process steps are not suitable to be relied upon if considering product claims. But it should also be acknowledged that *Vepa et al.* do not teach

the roughness claimed in the patent application and that even the combined documents of *Wilson et al* and *Vepa et al.* do not suggest the invention. This is because both lack any reference to an additional smoothing step the wafer is subjected to in order to achieve the claimed roughness.

As stated by *Vepa* on page 4 in lines 8 to 14, the surface roughness ranges between 1.2 nm to 2.0 nm. This prior art range does not overlap the claimed range of 0.05 to 0.29 nm RMS for the surface roughness. Then on page 4 in line 35 of *Vepa*, the surface roughness is stated to be reduced to the range of about 0.5 to about 0.8 nm. Hence, even this reduced range of *Vepa* fails to overlap the claimed range of 0.05 to 0.29 nm RMS for the surface roughness.

Hence, this Final Office Action in combining these prior art references to *Wilson* and *Vepa* fails to provide a prima facie case of obviousness. This is because no combination of these prior art references teaches all of the claimed limitations specified by the elected claim 1. Due to these clearly evident deficiencies in the teachings of the prior art references, there can be no anticipation of the present invention, and elected claim 1 is respectfully submitted to be patentable over the prior art applied under 35 U.S.C. 103.

The contention of the Patent Examiner that the *Vepa* surface roughness of not greater than 1.0 nm teaches the present invention is respectfully traversed. (See *Vepa* page 4, line 34). The *Vepa* surface roughness of not greater than 1.0 nm only refers to, and only suggests, the preferred range in *Vepa* of 0.5 to 0.8 nm. Nothing in *Vepa* suggests a surface roughness below, or less than, the lower limit of 0.5 nm of the *Vepa* range of 0.5 to 0.8 nm. Hence the lower range limit in *Vepa* of 0.5 nm does not teach the claimed range of 0.05 to 0.29 nm RMS.

The importance of the claimed range of 0.05 to 0.29 nm RMS is shown in the examples in the present Specification. In the Comparative Example 1 on page 19 of the Specification, the wafer surface had a roughness of 0.7nm RMS, and without the pretreatment of the invention, following the epitaxial coating on the front surface, had 0.52 LLS/cm^2.

On the other hand, referring to Example (Invention), the wafer surface roughness of 0.7 nm was reduced by pretreatment down to 0.17 nm RMS. Then after an epitaxial coating was applied to this pretreated surface, the total number of light defects was reduced to 0.03 LLS/cm^2.

Thus it is respectfully submitted that the combined

teachings of *Wilson* and *Vepa* would produce a wafer with a surface having 0.52 LLS/cm^2 rather than a wafer with the claimed surface of the epitaxial layer having a maximum density of 0.14 LLS/cm^2

In summary, elected claim 1, and the present invention, are patentable over all the prior art applied by the Patent Examiner. A prompt notification of allowability is respectfully requested.

Respectfully submitted,

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Enclosure: 1) One Sheet of Formal Drawings
2) Copy of Petition for One Month Extension of Time for Large Entity

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231, on March 5, 2003.

Maria Guastella

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APPLICANT:SIEBERT ET AL -2 EXAMINER:S.RAO
SERIAL NO: 09/716,708 GROUP: 2814
FILED: NOVEMBER 20, 2000
TITLE: EPITAXIALLY COATED SEMICONDUCTOR WAFER AND PROCESS FOR PRODUCING IT

COLLARD & ROE,P.C. 516-365-9802
SHEET 1 OF 1

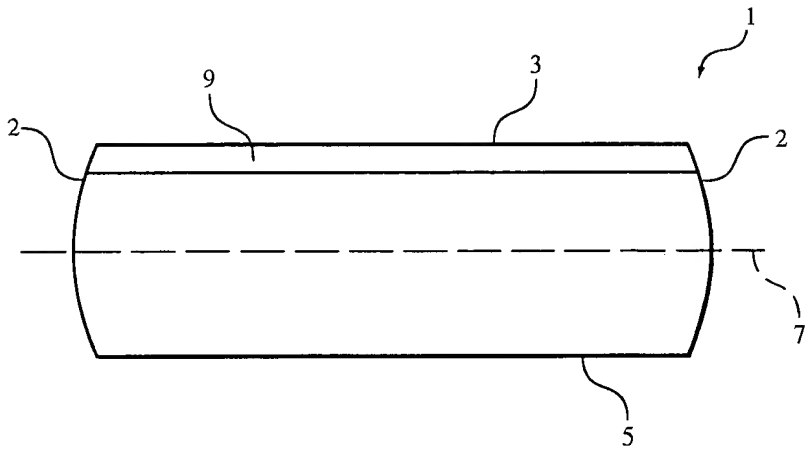

FIG. 1